REMARKS

The Final Office Action mailed April 6, 2005, has been received and reviewed. Claims 17 through 26, and 46 through 50 are currently pending in the application. Claims 46 through 50 stand rejected.

Amendment to the Specification

Applicants propose herein an amendment to the specification in the form of a reference to the parent reissue application (now RE 36,518) pursuant to M.P.E.P. 1451. Applicant asserts that this amendment is a requirement of the Office, and not an "error" requiring correction.

Applicants also note that a similar notice referencing the present application was not entered in the parent application hereto during pendency thereof and so is not in the text of the printed reissue patent, and respectfully requests that he submit this issue to his SPE, also pursuant to M.P.E.P. 1451, for inclusion of a Certificate of Correction and other associated action as set forth in the referenced M.P.E.P. section in the parent reissue patent hereto.

The Outstanding Final Office Action

The Final Office Action required in response thereto to secure allowance of the application the filing of a supplemental reissue oath or declaration covering claims 46 through 50 averring that all errors being corrected in the reissue application arose without any deceptive intention on the part of the applicants.

Applicants submit herewith in response to the Final Office Action, a Supplemental Reissue Declaration executed by inventor Guy T. Blalock averring that every error in the patent being corrected in the present reissue application, and which is not covered by the prior oath and/or declaration, arose without any deceptive intention on the part of the applicants.

The inventor Charles H. Dennison has refused to sign the Supplemental Declaration, as evidenced by the accompanying DECLARATION OF JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION.

This paper is submitted in response to a Final Office Action mailed on April 6, 2005 by Examiner Kevin M. Picardat. The relevant background facts are set forth below, as is a Petition to Suspend or Waive the Rules Pursuant to 37 C.F.R. 1.183.

Statement of Facts

Applicant's attorney forwarded a supplemental reissue declaration to Micron Technology, Inc. for execution by the inventor Guy T. Blalock. Mr. Blalock executed the Supplemental Reissue Declaration, the original of which is enclosed herewith.

Applicant's undersigned attorney knew that the inventor Charles H. Dennison had left the employ of Micron Technology, Inc. and now resides in San Jose, California in the employ of Ovonyx, Inc., a competitor with some product lines under development by the Assignee of the present application, Micron Technology, Inc.

To summarize the current situation, the inventor Charles H. Dennison was reached by email on May 2, 2005 with attachments including a supplemental reissue declaration, as set forth in more detail in the accompanying DECLARATION OF JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION.

On May 16, 2005, the undersigned contacted Mr. Dennison by telephone at his place of business, Ovonyx, Inc. regarding whether Mr. Dennison had received the email and attachments and whether he would sign the supplemental reissue declaration. Mr. Dennison, who is known personally to the undersigned, acknowledged receipt of the email and attachments and stated that he would not sign the supplemental reissue declaration.

Petition for Suspension or Waiver of the Rules Pursuant to 37 C.F.R. 1.183

Accordingly, Applicants herein respectfully petition for suspension or waiver of the rules pursuant to 37 C.F.R. 1.183, and specifically for a waiver of the requirement for a Supplemental Reissue Declaration executed by inventor Charles H. Dennison he has refused to execute and return to Applicants' attorney the Supplemental Reissue Declaration received by him on May 2, 2005. Applicant also relies upon M.P.E.P. 1414.01 as authorizing the filing of this petition as an appropriate response in the present circumstances.

Applicants submit herewith in response to the Final Office Action of April 6, 2005:

1) DECLARATION OF JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION with attached Exhibits A through E;

2) REQUEST FOR TRANSFER OF SURRENDERED ORIGINAL PATENT;

3) a Supplemental Reissue Declaration executed by the inventor Guy T. Blalock averring that every error in the patent being corrected in the present reissue application, and which is not covered by the prior oath and/or declaration, arose without any deceptive intention on the part of the applicants; and

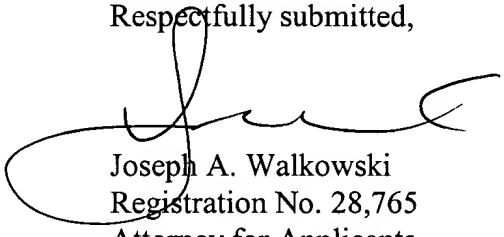
4) The required fee under 37 C.F.R. 1.17(h) in support of the suspension or waiver of the rules pursuant to 37 C.F.R. 1.183; and

The Office is hereby authorized to charge any additional fees required to Deposit Account No. 20-1469.

CONCLUSION

Applicants respectfully request prompt and favorable action, and issuance of a Notice of Allowability with an accompanying Notice of Allowance and Fee(s) Due. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: May 26, 2005
JAW/dlm:slm

Document in ProLaw

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 09/488,099

Filed: January 18, 2000

For: METHOD FOR MAKING ELECTRICAL CONTACT WITH AN ACTIVE AREA THROUGH SUB-MICRON CONTACT OPENINGS AND A SEMICONDUCTOR DEVICE

Confirmation No.: 3941

Examiner: K. Picardat

Group Art Unit: 2822

Attorney Docket No.: 2269-3255.1US
(91-0507.01/RE)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

May 26, 2005
Date

Signature

Joseph A. Walkowski
Name (Type/Print)

DECLARATION BY JOSEPH A. WALKOWSKI REGARDING REFUSAL OF CHARLES H. DENNISON TO EXECUTE SUPPLEMENTAL REISSUE DECLARATION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I am a shareholder and director of the law firm of TraskBritt, P.C., located at 230 South 500 East, Suite 300, Salt Lake City, Utah 84102, Reg. No. 28,765.

I am an attorney of record in the above-referenced application.

I know the inventor Charles H. Dennison personally, having worked with him in the context of preparing and prosecuting patent applications with which he was involved as an

inventor while he was in the employ of the Assignee of the present application, Micron Technology, Inc. in my capacity as outside counsel to Assignee. Mr. Dennison left the employ of Micron Technology, Inc. a number of years ago and is now in the employ of Ovonyx, Inc., a competitor of some product lines under development by the Assignee.

On May 2, 2005, I sent Mr. Dennison an email, a true copy of which is attached hereto as Exhibit A, requesting that he execute a Supplemental Reissue Declaration (Exhibit B). I also forwarded him a copy of original U.S. Patent 5,229,326 (Exhibit C), parent reissue U.S. Patent RE 36,518 (Exhibit D) and the pending claims of the present application (Exhibit E) for his reference.

On May 16, 2005 I called Mr. Dennison at his place of business, reached him at his desk, and asked 1) had he received my email of May 2, 2005 with the attachments, and 2) was he going to execute the proffered Supplemental Reissue Declaration. Mr. Dennison acknowledged receipt of the email and attachments, politely but unequivocally refused to execute the Supplemental Reissue Declaration, and the conversation was terminated.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

May 26, 2005
Date

Joseph A. Walkowski

Document in ProLaw

Joseph Walkowski

From: Joseph Walkowski
Sent: Monday, May 02, 2005 10:47 AM
To: 'cdennison@ovonyx.com'
Subject: Another Micron reissue application

Dear Chuck,

Per my earlier email this morning, we have another Reissue continuation application, Serial No. 09/488,099, in which we are required to file a Supplemental Reissue Declaration. You and Guy Blalock are the inventors on this application.

I enclose for your review:

1) A PDF copy of the original U.S. Patent 5,229,326
2) A PDF copy of the first Reissue Patent RE 36,518 (which includes the claims from the '326 patent
3) A Word copy of the pending claims (allowed, but for the lack of a Supplemental Reissue Declaration) for application Serial No. 09/488,099 which is a continuation of #2. The specification and drawings are the same as in #1 and #2 above, so I am not sending these.
4) A Word copy of the Supplemental Reissue Declaration

As with the other matter, I would appreciate you signing, dating and forwarding the executed declaration document back to me at your earliest convenience.

If you would sign the Supplemental Reissue Declaration and fax it back to me at 801-531-9168 or scan it and send it as an email attachment, it would be most appreciated. If you have questions, I will be back in the office on May 5th, and please feel free to call me at 1-800-900-2001 or email me and I will respond upon my return.

Thank you for your assistance and, again, I apologize for the imposition.

Joe Walkowski


US05229326.pdf (577 KB)


RE36518.PDF (745 KB)


Pending Claims.doc (42 KB)


Supplemental Reissue Declarati...

Exhibit A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Dennison et al.

Serial No.: 09/488,099

Filed: January 18, 2000

For: METHOD FOR MAKING ELECTRICAL CONTACT WITH AN ACTIVE AREA THROUGH SUB-MICRON CONTACT OPENINGS AND A SEMICONDUCTOR DEVICE

Confirmation No.: 3941

Examiner: K. Picardat

Group Art Unit: 2822

Attorney Docket No.: 2269-3255.1US
(91-0507.01/RE)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date _____ Signature _____

Joseph A. Walkowski
Name (Type/Print)

SUPPLEMENTAL REISSUE DECLARATION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We hereby declare that:

Every error in the patent which was corrected in the present reissue application up to the time(s) of execution of this declaration by each of us, and which is not covered by the prior oath(s) and/or declaration(s) submitted in this application, arose without any deceptive intention on the part of the applicants.

Exhibit B

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: _____ _____

Charles H. Dennison

Inventor's Full Name:	Charles H. Dennison
Country of Citizenship:	United States of America
Residence Address:	5719 Algonquin Way San Jose, California 95138
Post Office Address:	same as above

Date: _____ _____

Guy T. Blalock

Inventor's Full Name:	Guy T. Blalock
Country of Citizenship:	United States of America
Residence Address:	8101 Slickwood Ct. Boise, Idaho 83704
Post Office Address:	same as above

Document in ProLaw

PENDING CLAIMS
Serial No. 09/488,099
TraskBritt Ref. No. 2269-3255.1US
Client Ref. No. 91-0507.01/RE

Claims 1-16 are canceled.

17. A semiconductor processing method of forming an electrical contact structure for an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the mutually adjacent sides of the conductive runners, the insulated mutually adjacent sides of adjacent conductive runners being spaced a selected distance apart;

providing an active area between the insulated mutually adjacent sides of conductive runners;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulated sides of adjacent conductive runners;

providing a first insulating layer having a planarized upper surface atop the first oxide layer, the first layer of insulating material being selectively etchable relative to the first oxide;

patterning the first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the first insulating layer planarized upper surface, the aperture width being greater than the selected distance between the insulated sides of adjacent conductive runners:

etching the first oxide layer within the first contact opening to expose the active area; and

providing a conductive plug of within the first contact opening over the exposed active area.

18. A semiconductor processing method according to claim 17 wherein the step of providing a plug of conductive material comprises:

providing a layer of conductive material over the first insulating layer and within the first contact opening over the exposed active area; and

polishing the wafer to remove the conductive layer from the first insulating layer planarized upper surface and to define the conductive plug within the first contact opening, the plug having an upper surface slightly below the first insulating layer planarized upper surface.

19. A semiconductor processing method according to claim 17 further comprising:

providing a second insulating layer and the conductive plug; and

patterning and etching the second insulating layer to form a second contact opening to expose the conductive plug.

20. A semiconductor processing method according to claim 19 further comprising etching the second insulating layer with an etchant selective to both the first insulating layer and the conductive plug.

21. A semiconductor processing method according to claim 19 further comprising:

forming the first insulating layer of a nitride;

forming the conductive plug of polysilicon; and

etching the second insulating layer with an etchant selective to both the nitride insulating layer and the polysilicon plug.

22. A semiconductor processing method of forming an electrical contact structure for an active area on a semiconductor wafer, the method comprising the following steps:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having sides;

providing an insulative layer on the mutually adjacent sides of the conductive runners, the insulated mutually adjacent sides of adjacent conductive runners being spaced a selected distance apart;

providing an active area between the insulated mutually adjacent sides of conductive runners;

providing a layer of first oxide to a selected thickness over the active area and conductive runners, the first oxide layer selected thickness being less than one-half the selected distance between the insulated sides of adjacent conductive runners;

providing a first insulating layer having a planarized upper surface atop the first oxide layer, the first insulating layer being selectively etchable relative to the first oxide, said step performed by,

providing a conformal first layer of insulating material atop the first oxide layers; and

polishing the wafer to planarize the first insulating layer upper surface;

patterning the first insulating layer for definition of a first contact opening therethrough to the active area;

etching the patterned first insulating layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the first insulating layer planarized upper surface, the aperture width being greater than the selected distance between the insulated sides of adjacent conductive runners;

etching the first oxide layer within the first contact opening to expose the active area; and

providing a conductive plug within the first contact opening over the exposed active area.

23. A semiconductor processing method for making electrical contact with an active area on a semiconductor wafer comprising the steps of:

providing a pair of conductive runners on a semiconductor wafer, individual conductive runners having a top and sides;

providing insulative spacers on mutually adjacent sides of the runners, the insulative spacers being spaced a selected distance apart at a selected location on the wafer;

providing an active area between the conductive runners at the selected location;

depositing a first oxide layer over the wafer to a thickness from about 100 to 1,000 Angstroms, the first oxide layer having an upper surface defining a highest elevational location above the active area;

providing a nitride layer having an upper surface over the first oxide layer to a selected thickness, the nitride layer upper surface defining a lowest elevational location above the active area which is elevationally higher than the highest elevational location of the first oxide layer, the nitride being selectively etchable relative to the first oxide;

planarizing an upper surface of the nitride layer to a first elevational height above the active area, the first elevational height being higher than the highest elevational location of the first oxide layer upper surface;

patterning the nitride layer for definition of a first contact opening therethrough to the active area;

etching the patterned nitride layer selectively relative to the first oxide layer to define the first contact opening therethrough, the first contact opening having an aperture width at the nitride layer upper surface which is greater than the selected distance between the insulative spacers at the mutually adjacent sides of the conductive runners;

etching the first oxide layer within the first contact opening to expose the active area;

providing a polysilicon plug within the first contact opening over the exposed active area to a second elevational height; and

depositing a second oxide layer over the nitride layer and the polysilicon plug.

24. A semiconductor processing method according to claim 23 wherein the step of planarizing the nitride layer comprises polishing the wafer to planarize the nitride layer.

25. A semiconductor processing method according to claim 23 wherein the step of providing a polysilicon plug comprises:

providing a layer of polysilicon over the nitride layer and within the first contact opening over the exposed active area; and

polishing the wafer to remove the polysilicon layer from the nitride layer upper surface and to define a polysilicon plug within the first contact opening.

26. A semiconductor processing method according to claim 23 further comprising etching the second oxide layer by an etchant selective to both the nitride layer and the polysilicon plug.

Claims 27-45 are canceled.

46. A method of providing electrical communication with a transistor including a source/drain, said method comprising:

providing a conductor over said source/drain that extends upward and is laterally surrounded by a first layer of insulation;

providing a second layer of insulation over said first layer of insulation, wherein said second layer of insulation is higher than said conductor and exposes said conductor; and

allowing electrical communication with said source/drain only by way of said conductor.

47. The method in claim 46, wherein said step of providing a conductor comprises providing a plug.

48. A method of processing a device comprising a transistor, said method comprising:
providing a plug in electrical communication with said transistor;
providing a conductive material in electrical communication with said plug; and
providing an insulating layer lateral to said conductive material, wherein said step of providing an insulating layer occurs before said step of providing a conductive material.

49. The method in claim 48, further comprising a step of providing a first insulating layer over said transistor; and wherein said step of providing an insulating layer lateral to said conductive material comprises providing a second insulating layer over said first insulating layer.

50. The method in claim 49, wherein said step of providing a conductive material is discrete from said step of providing a plug.